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Advantages of linear amplifiers in Power Hardware In the Loop applications

Structure

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2. Definition PHIL
3. Principles of linear power amplifiers
4. Advantages of linear power amplifiers in PHIL applications
5. Example and measurements
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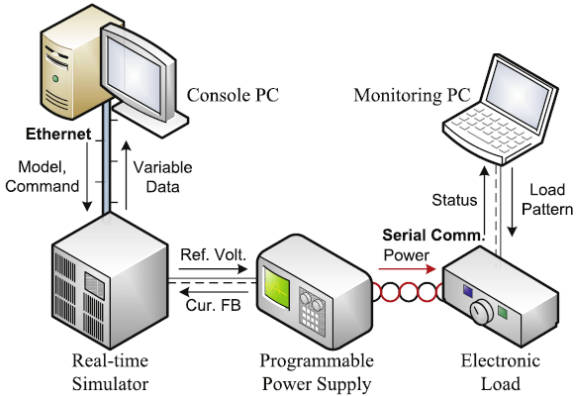


Advantages of linear power amplifiers for PHIL?

Introduction

PHIL simulations have to be stable and accurate!

Problems:

- Only low dynamic simulations due to stability problems of PHIL simulation system possible
- Loss of time and money due to inaccuracy of simulation

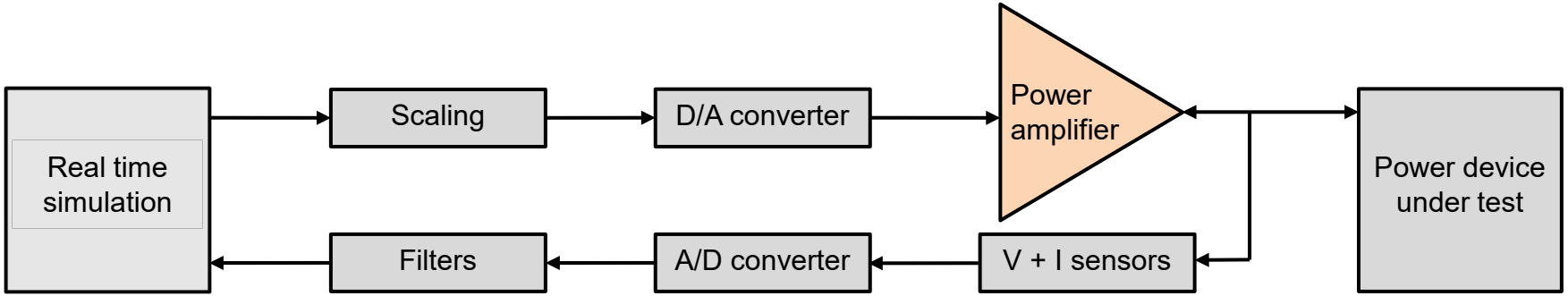
Definition PHIL

- **P**ower **H**ardware **I**n the **L**oop (PHIL)

  Power Hardware-in-the-Loop (PHIL) simulation represents a natural extension of HIL, in which the real-time simulation environment is capable of exchanging not just low-voltage, low-current signals, but the power required by the Devices under Test (DUT).

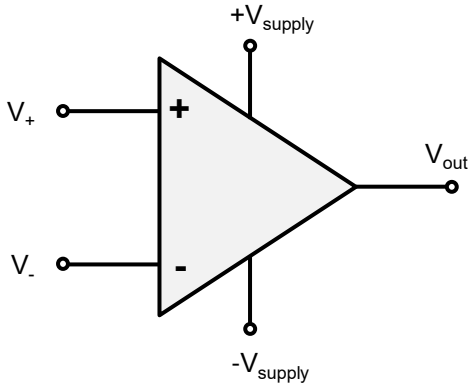
  ⇒ Necessity for power amplifiers

Schematic diagram for PHIL



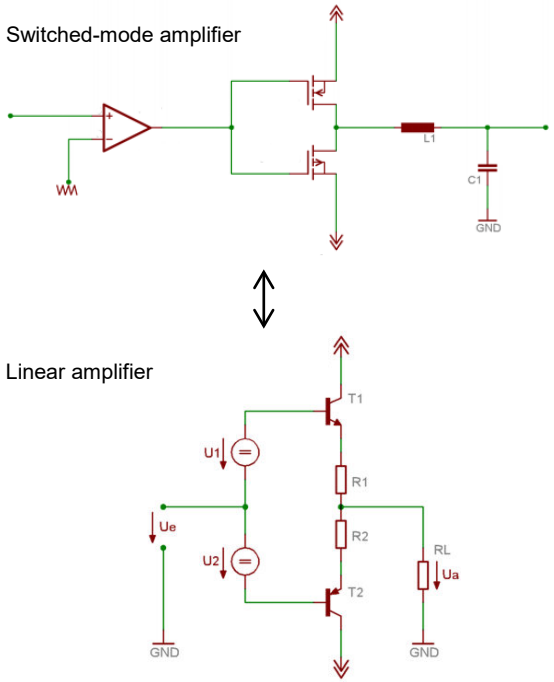
Selection of the amplifier for PHIL application

- Source and sink power ratings of the amplifier
- Power ratings of the device under test
- Amplifier interface connections
- Amplifier input and output voltage/current range
- Amplifier input and output impedances
- Amplifier protection (overload, heating, short circuit)
- Amplifier harmonic distortion and frequency resolution
- Amplifier delay time
- Amplifier slew rate

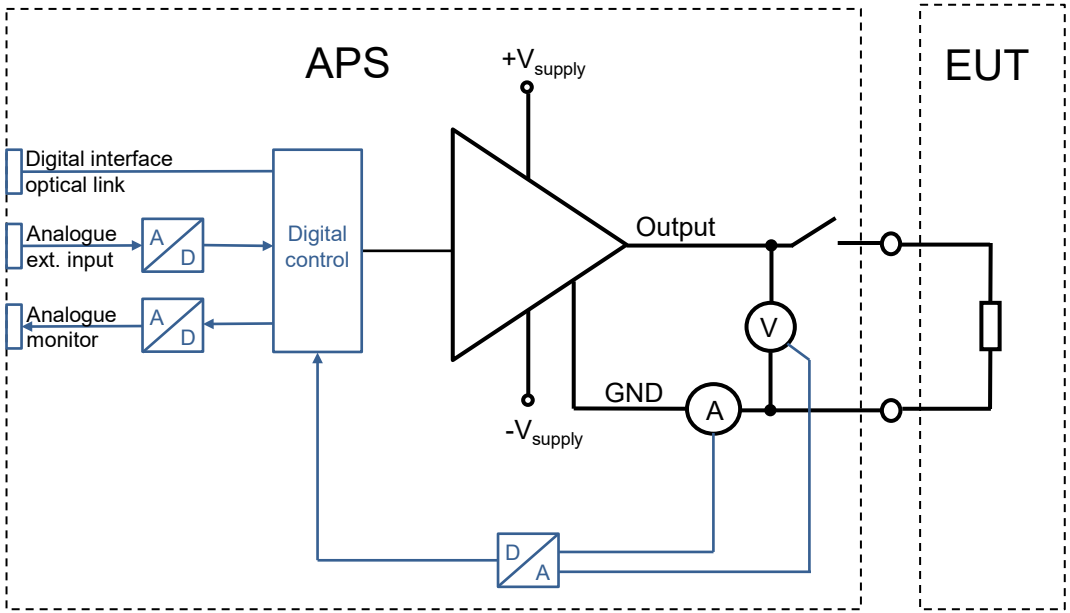


Comparison of switched-mode with linear amplifiers

	Switched-mode amplifier	Linear amplifier
Bandwidth	reduced bandwidth	high bandwidth
Delay time	long delay time	short delay time
Efficiency	high	medium
Application range	commonly used in MW range	< MW
Cost	medium	high
Peak current	low	high
Output noise	medium	low



Principle of linear power amplifier APS



Technical data of APS

Interfaces
LAN, GPIB, RS232

Power ratings
1kVA … 1MVA

Voltage
0V … 1500V

Slew rate
> 52V/µs

Current
0A … 10.000A

Delay time
≈ 5-10µs

Bandwidth
DC … 30kHz

Harmonic distortion
< 0.2%

Protection
Overload, short-circuit, overtem-perature

Output impedance
< 5mΩ

Features of APS

Large signal bandwidth DC … 30kHz

Small signal bandwidth up to 100kHz

High dynamic voltage and current limitation

Very high peak-load ability (up to 3ms)

4-quadrant operation mode

High short-term overload characteristic

Voltage and current mode operation

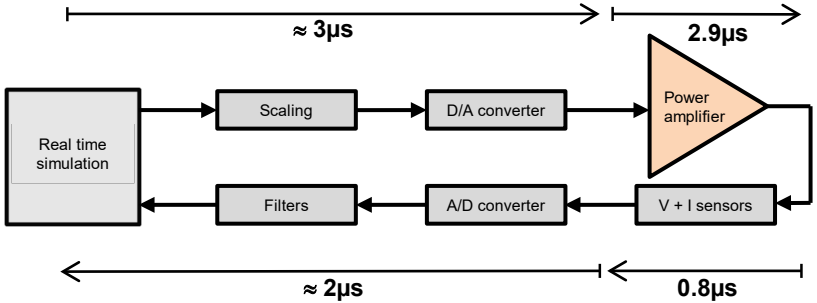
Extremely low harmonic distortion

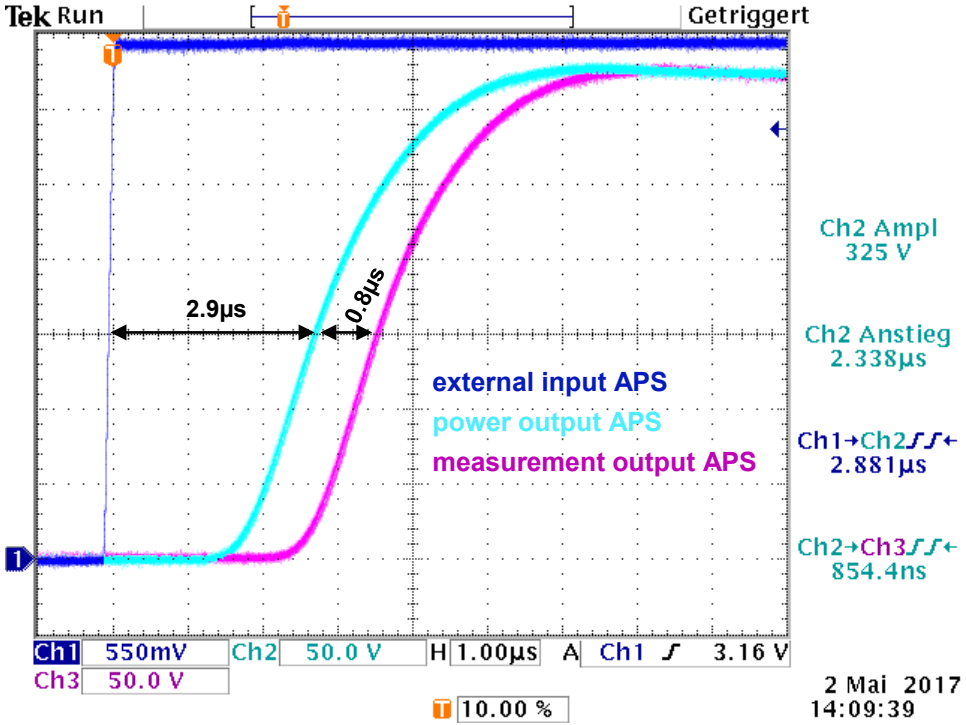
Very fast slew rate
⇒ Rise time < 5µs
(IEC 61000-4-11)

Very low internal resistance

Delay time of analogue interface (without load)

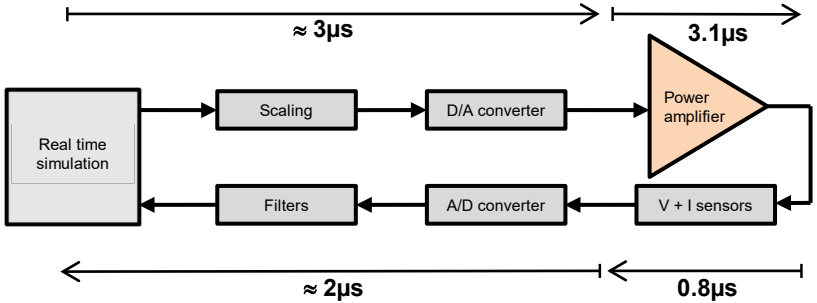
- Delay time between external analogue input and power output APS: 2.9µs
- Delay time between power output and measurement output APS: 0.8µs
- Additional time delay for output real-time simulator and read measurement: ≈ 5µs

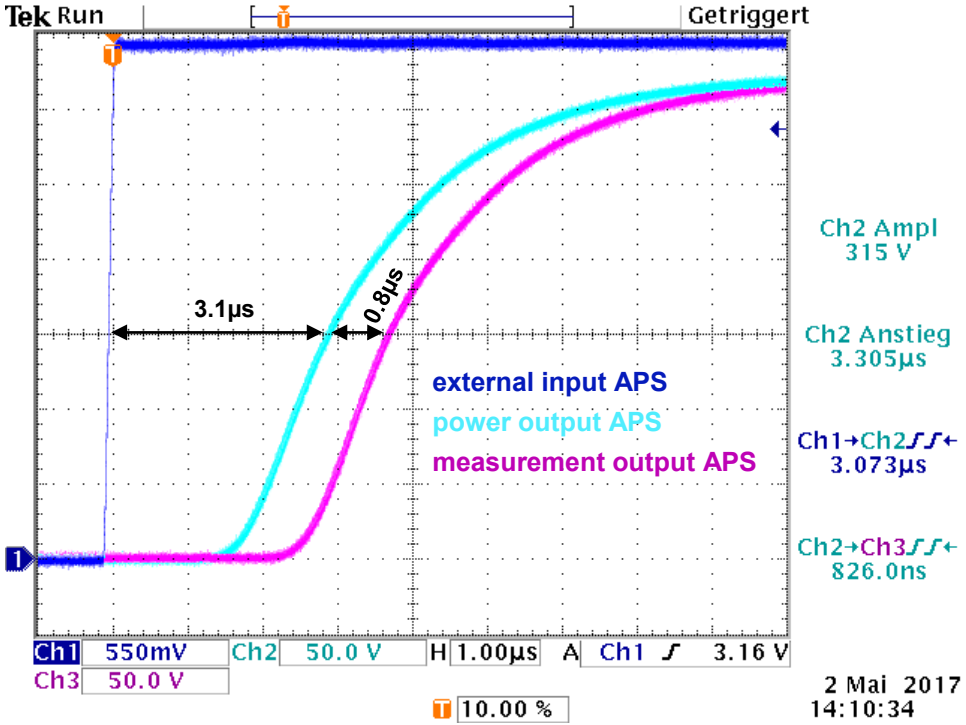




Delay time of analogue interface (with 100Ω load)

- Delay time between external analogue input and power output APS: 3.1µs
- Delay time between power output and measurement output APS: 0.8µs
- Additional time delay for output real-time simulator and read measurement: ≈ 5µs



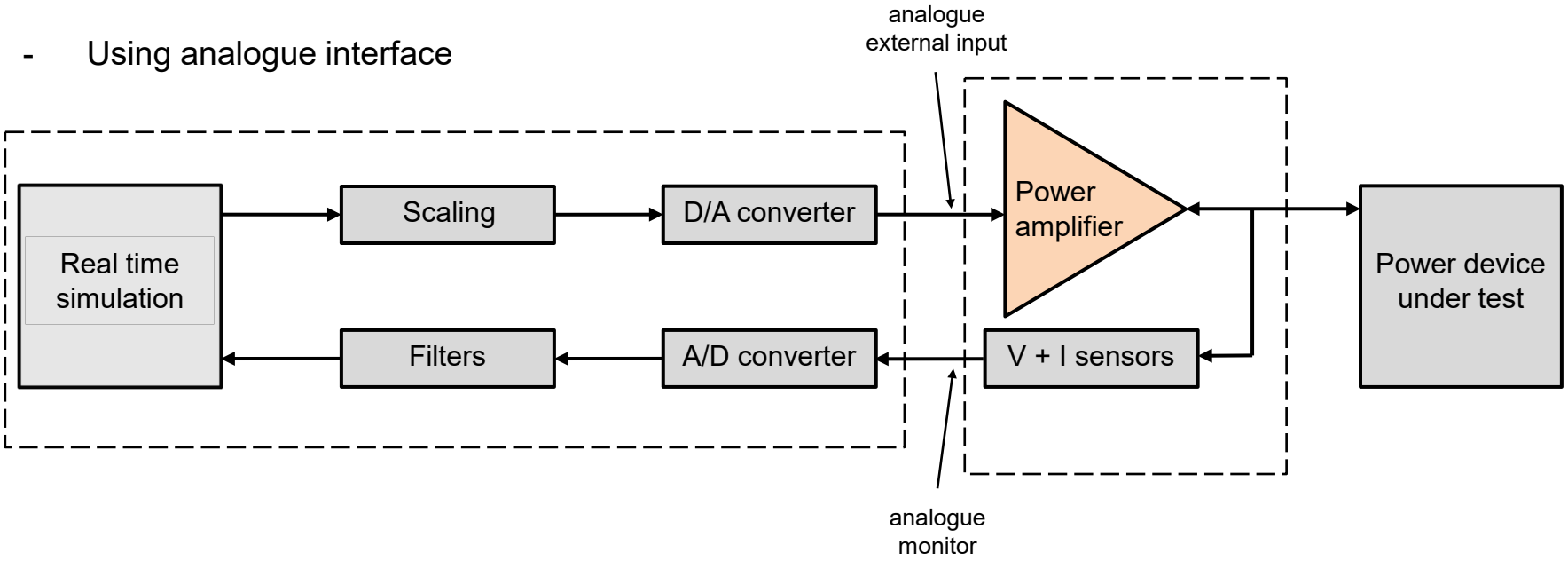


Technical data of monitor output APS

Monitor output	Voltage V	Current I
Measuring ranges	$900V_p$ / $450V_p$ / $225V_p$ / $112.5V_p$	depending on peak current of the amplifier
Max. amplitude	$\pm 10V_p$	
Scaling	0.2 … 1000	0.1 … 1000
Bandwidth	300kHz	200kHz
Accuracy	0.3%	
Noise of ADC measurement	$<20mV_{rms}$ (DC ... 300kHz)	$<1.5mA_{rms}$ (DC ... 300kHz)
Noise of DAC output	$<0.2mV_{rms}$ (DC ... 300kHz)	$<0.2mV_{rms}$ (DC ... 300kHz)
Delay time	<1µs	
Output impedance	47Ω	
Isolation	isolated against each other, against remaining electronics and against earth	
Protection	Short circuit	

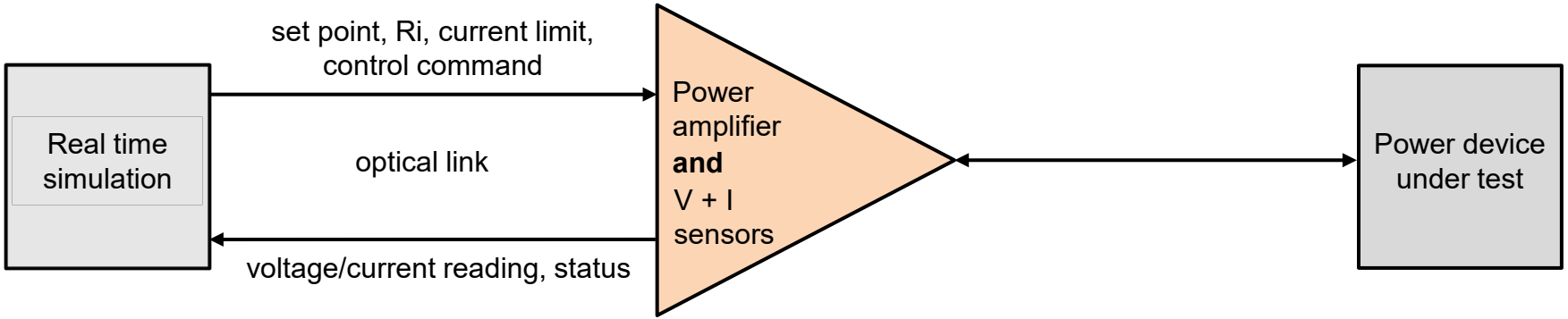
Principle schematic for PHIL

- Using analogue interface



Principle schematic for PHIL

- Using digital interface



No delay and accuracy loss
due to D/A and A/D conversion!

Optical link between RTS and linear power amplifier

- Hardware: High-speed optical serial transceivers 2x7 SFF 850nm
- Protocol: Xilinx® LogiCORE™ IP Aurora 8B/10B
- Data Rate: 2Gb/s
- Transmission: Easy-to-use AXI4-Stream based framing 4-byte-per-lane
- CRC: 32-bit
- Flow control: None
- Protocol data:

Rx_D:

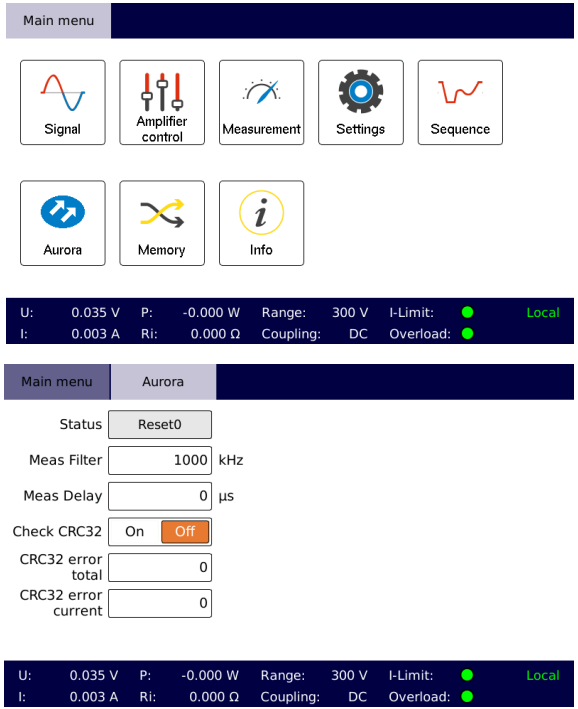
Set point	Maximum current limitation	Minimum current limitation	Internal resistance	Command value	Echo request	CRC

Tx_D:

Voltage reading	Current reading	Status value	Echo response	CRC

Advantages of optical link

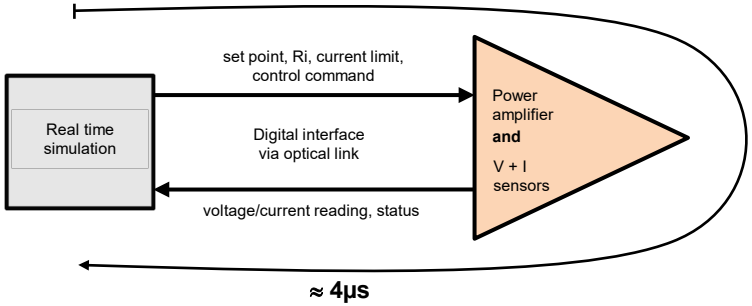
- Less time delay
- Higher accuracy due to unnecessity of AD and DA conversion
- No interference due to electric or magnetic field (no additional noise)
- Possibility of high distance between simulator and amplifier (maximum link length > 100m)
- Integrated digital measuring filter
- Simpler design / no complex physical wiring
- Plug and Play
- Lower costs
- Available for OPAL-RT and RTDS simulator



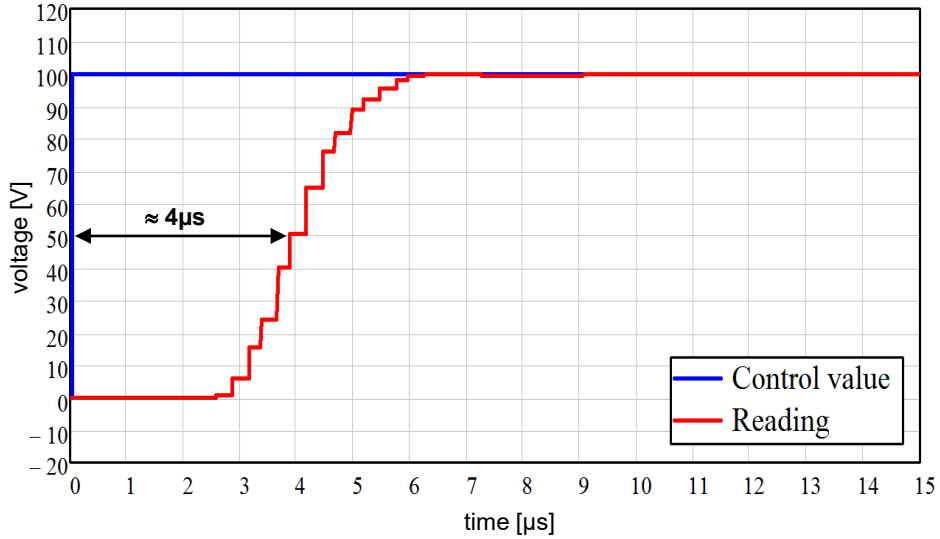
Delay time of digital interface via optical link

- Step response measurement

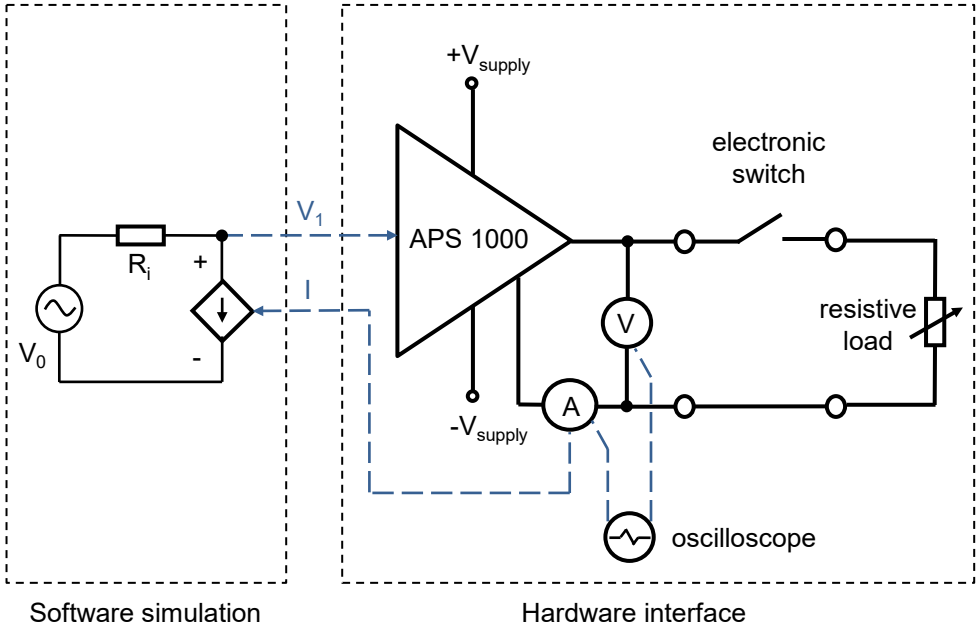
  Delay time between send digital control value and receive digital reading: ≈ 4µs

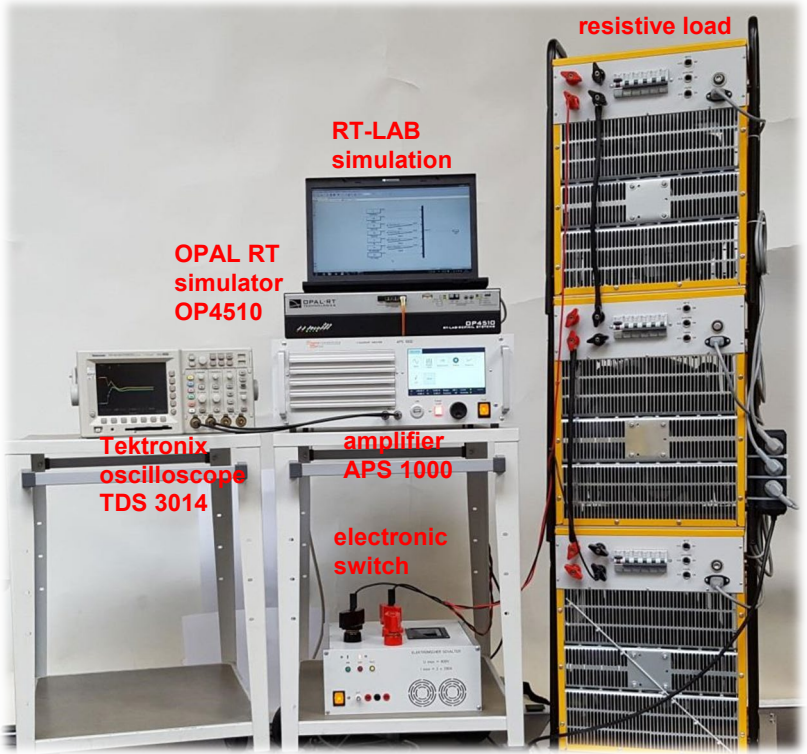


Step response of digital control



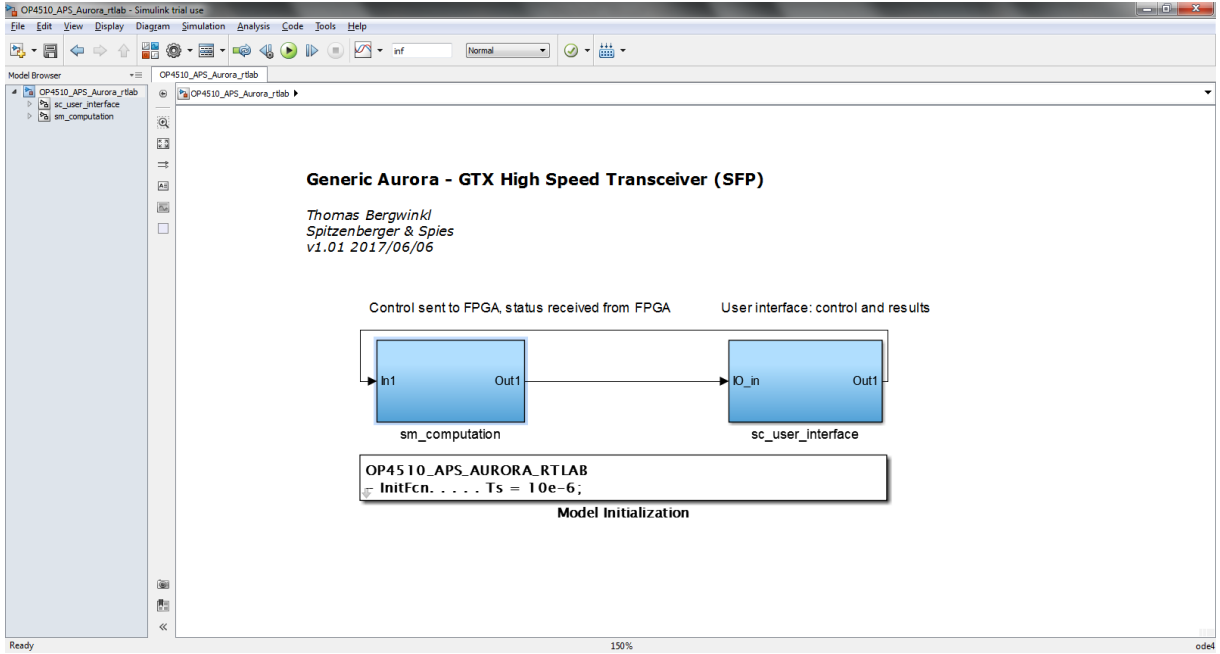
Example PHIL test setup





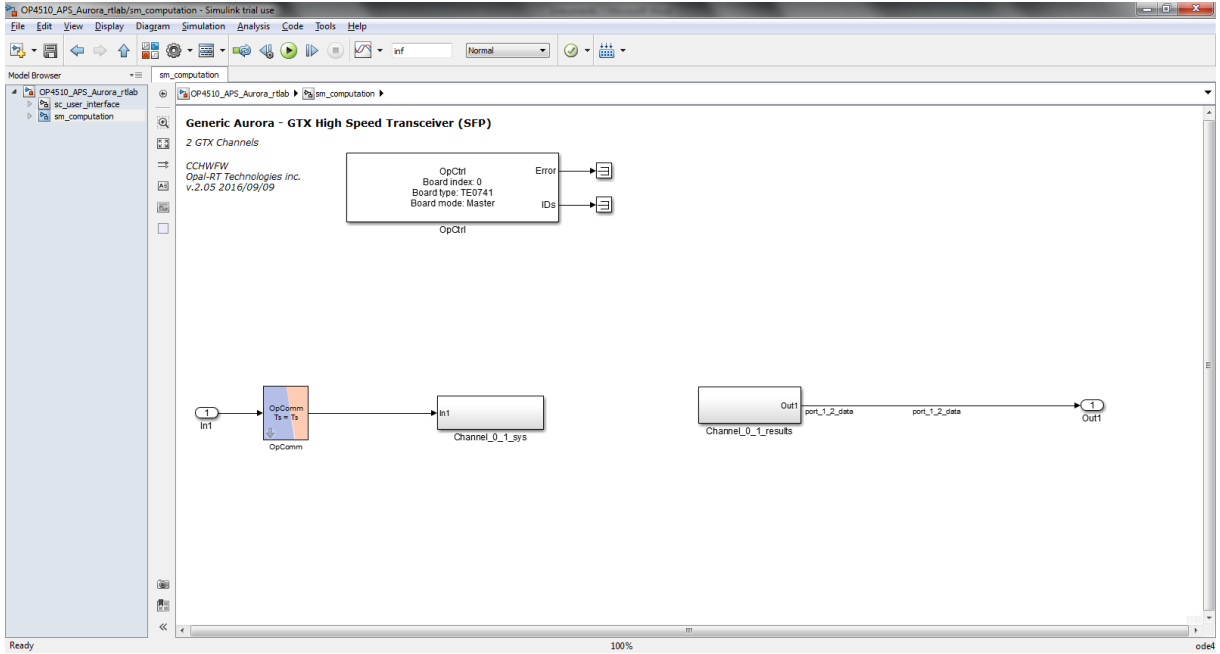
Example project: Simulation of power source with internal resistance

- Top level of example project
- Model consists of computation block and user interface for setting input values
- Time step is set to 10ns



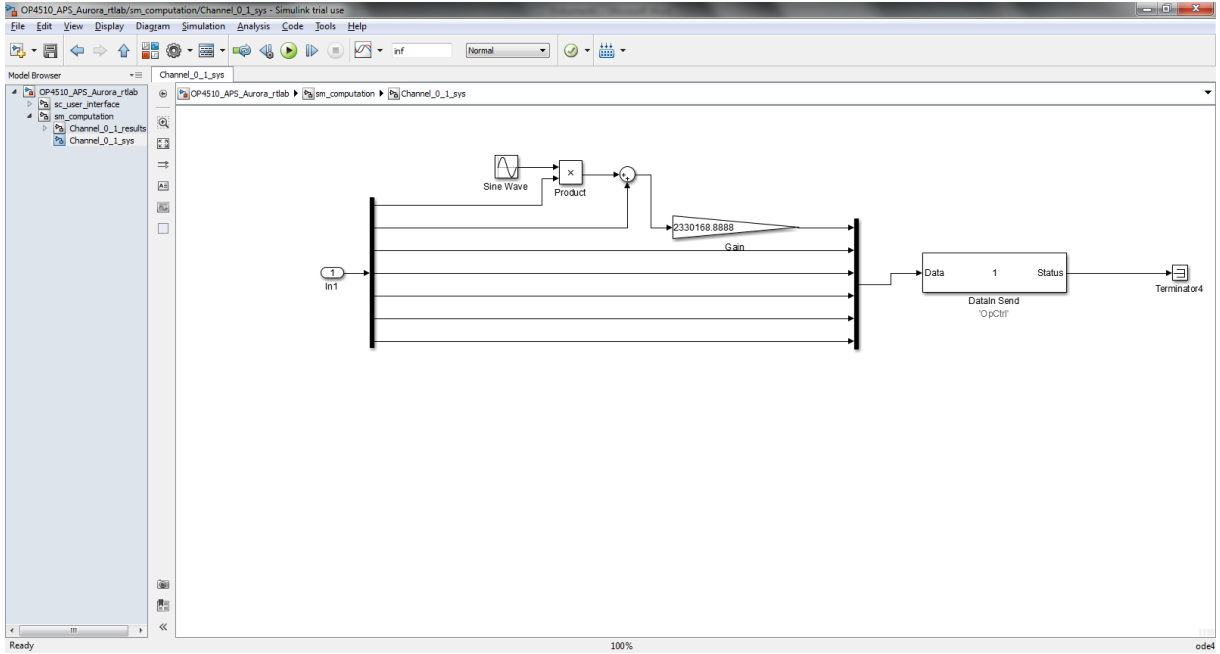
Example project: Simulation of power source with internal resistance

- Block sm_computation consists of an input from user interface and an output to user interface
- Computation is done within CPU



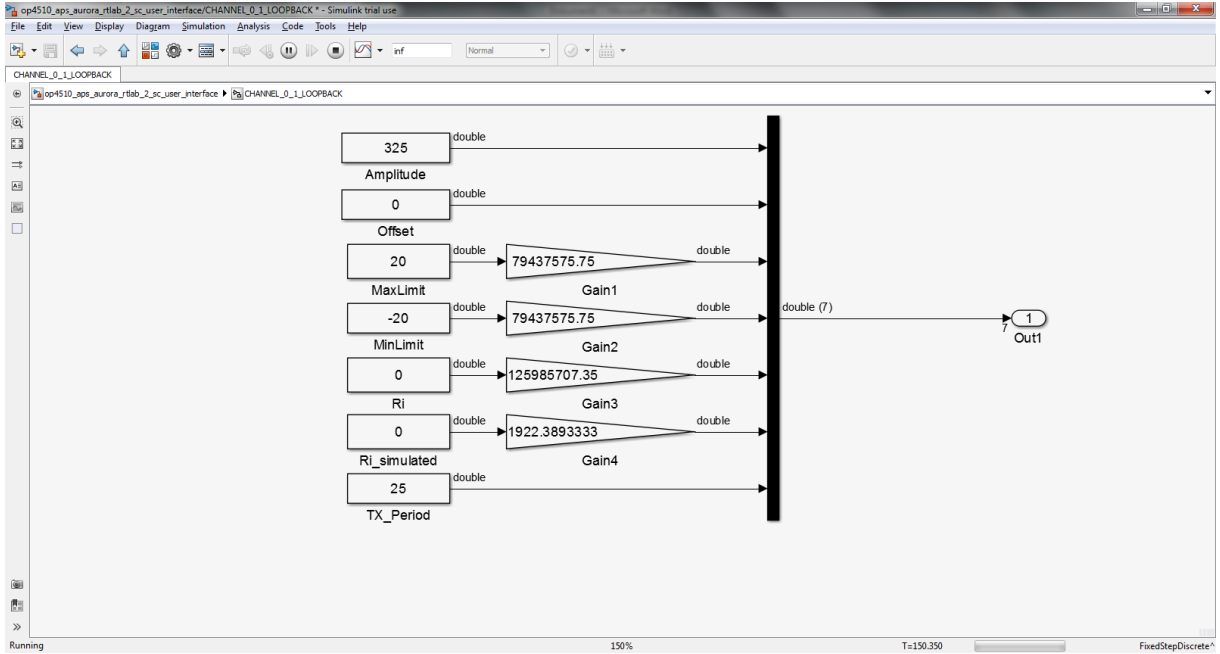
Example project: Simulation of power source with internal resistance

- Block Channel_0_1_sys contains the generation of a sine wave with constant frequency which is multiplied with the amplitude factor and added to an offset from the user interface
- PXI interface to FPGA
- $Gain = \frac{2^{31}}{\frac{1024}{1000} * 900V} = 2330168.8888$



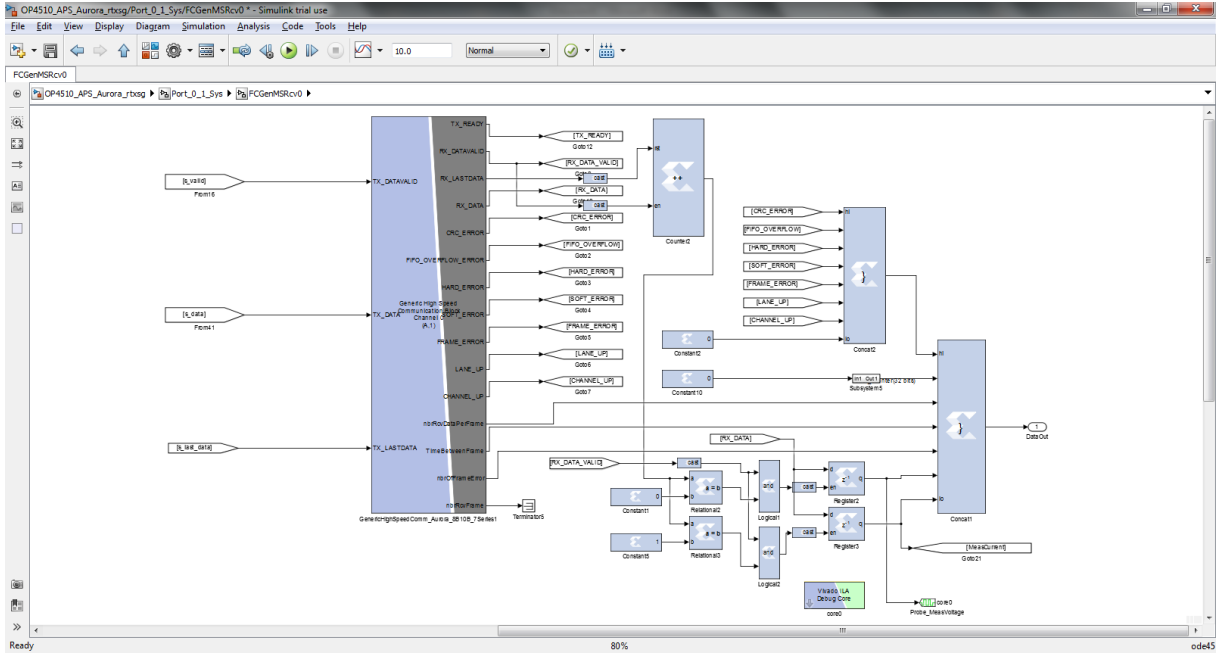
Example project: Simulation of power source with internal resistance

- Block sc_user_interface consists of an input from FPGA and an output to FPGA
- Computation is done within CPU
- *Gain1 = Gain2* $= \frac{2^{31}}{\frac{1024}{1000} * 26.4A} = 79437575.75$
- *Gain3* $= \frac{2^{32}}{\frac{900V}{26.4A}} = 125985707.35$
- *Gain4* $= \frac{2^{16}}{\frac{900V}{26.4A}} = 1922.3893333$



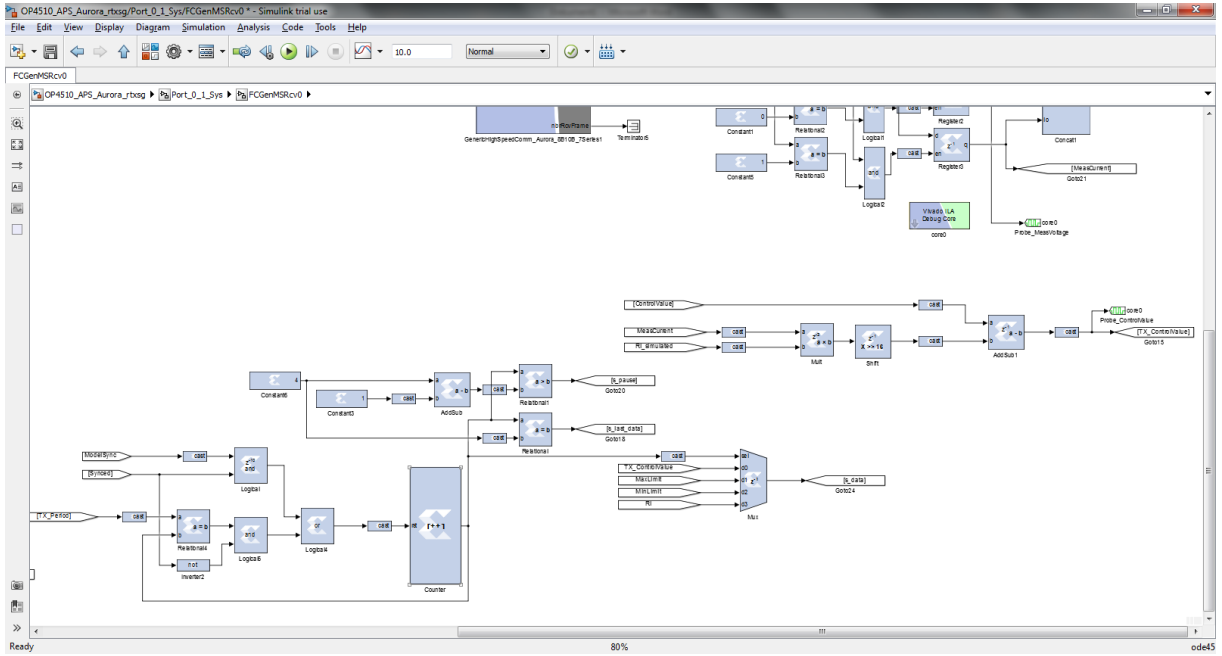
Example project: Simulation of power source with internal resistance

- FCGenMSRcv0 contains the Aurora protocol and the internal resistance simulation
- Computation is done within FPGA



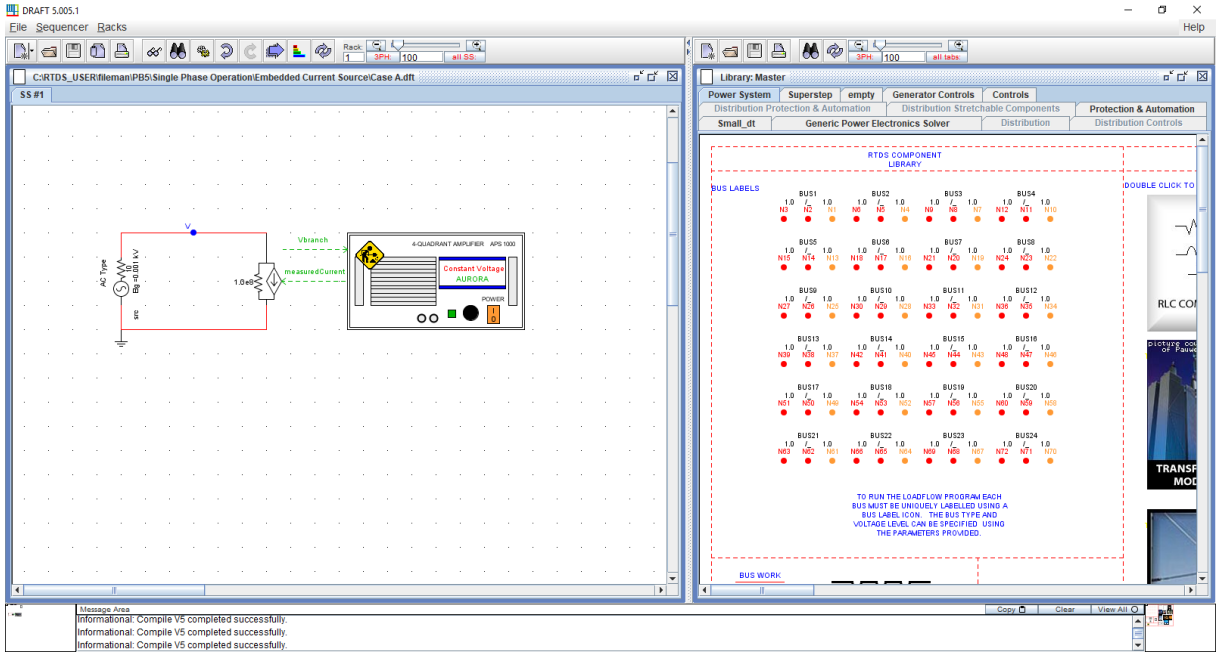
Example project: Simulation of power source with internal resistance

- FCGenMSRcv0 contains the time step adjustment
- Computation is done within FPGA



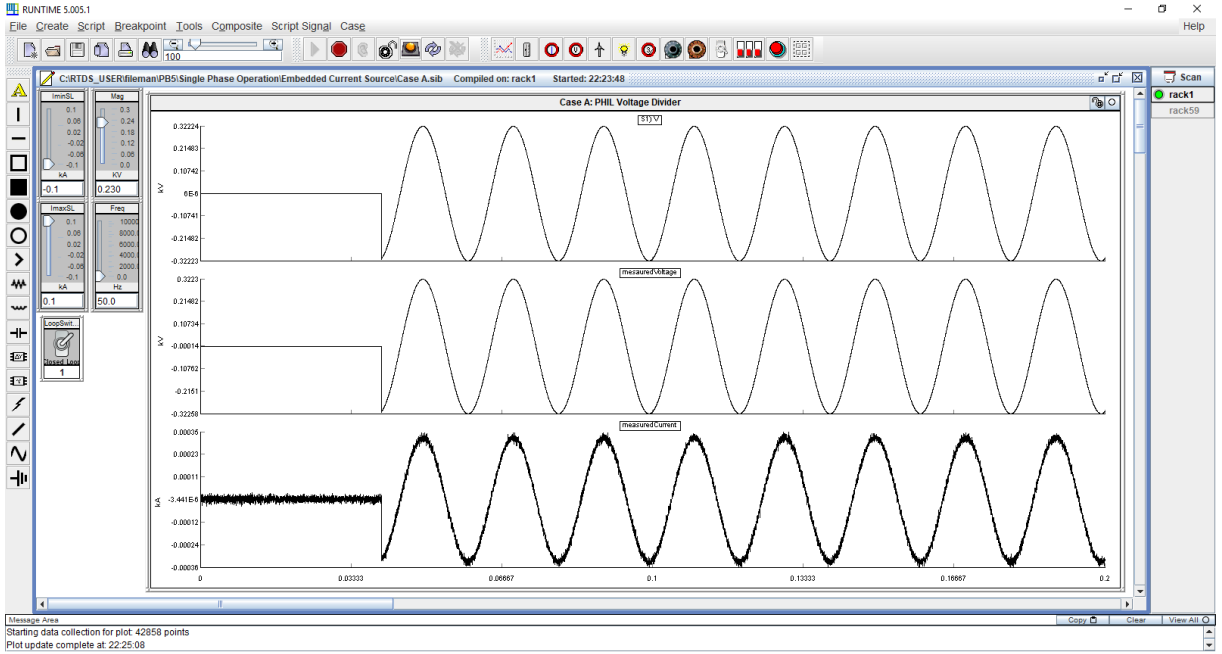
Example project: Simulation of power source with internal resistance

- _rtds_Aurora_SPS_Inj component can be used for optical link connection
- Selection options: voltage or current source

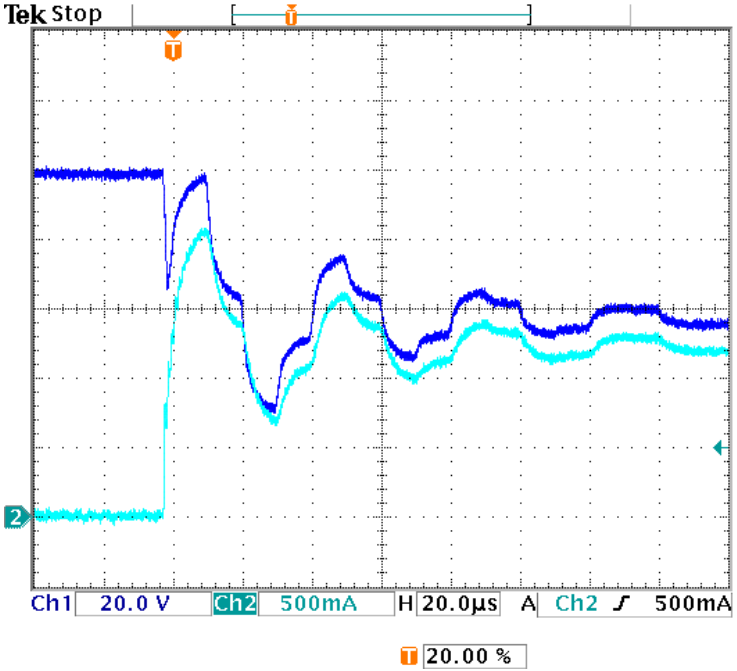


Example project: Simulation of power source with internal resistance

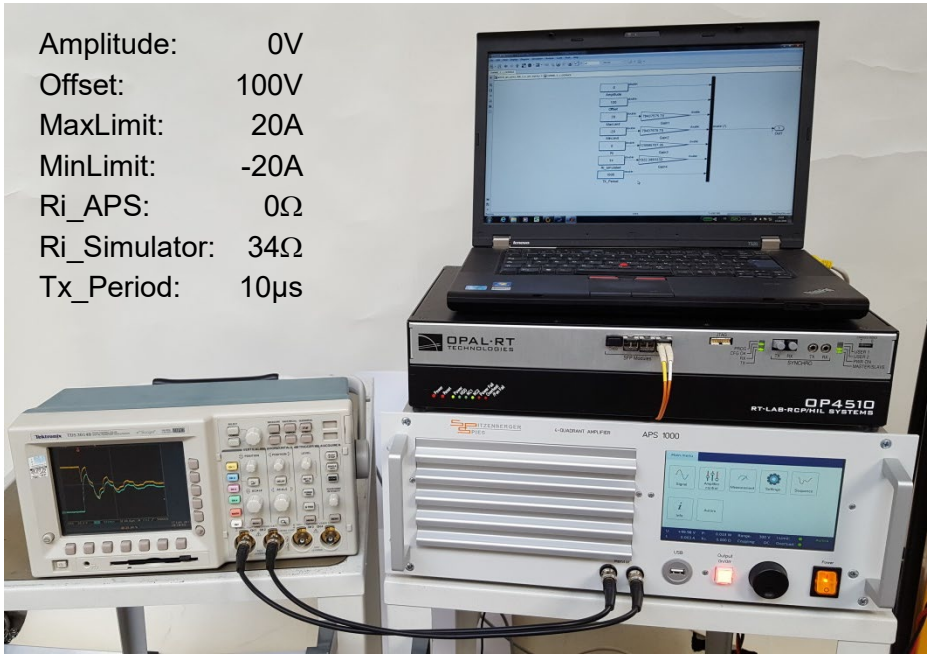
- Parameter setting by slider or numerical value
- Graphic representation of set point values and readings



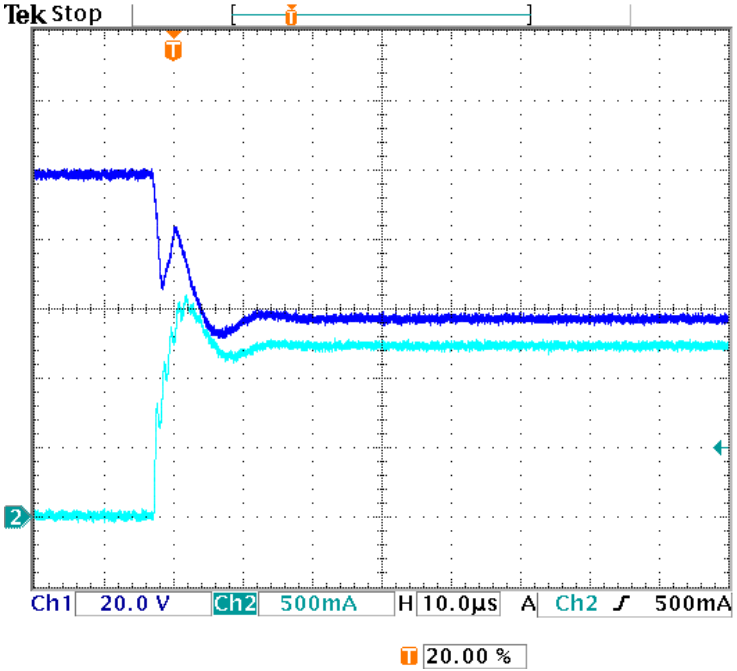
Simulation of internal resistance with RT simulator (10µs time steps)

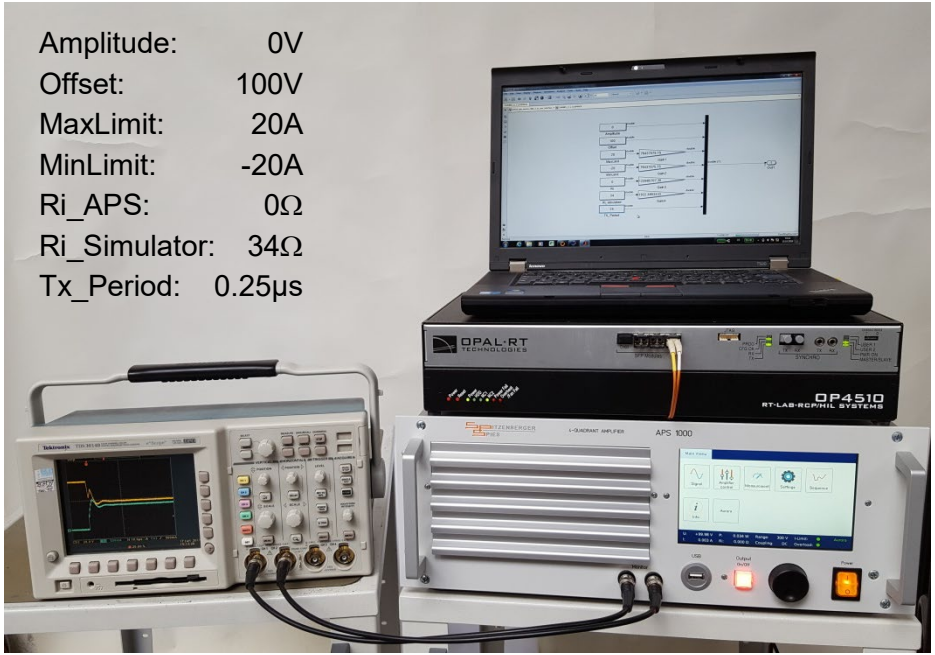


Amplitude: 0V
Offset: 100V
MaxLimit: 20A
MinLimit: -20A
Ri_APS: 0Ω
Ri_Simulator: 34Ω
Tx_Period: 10µs

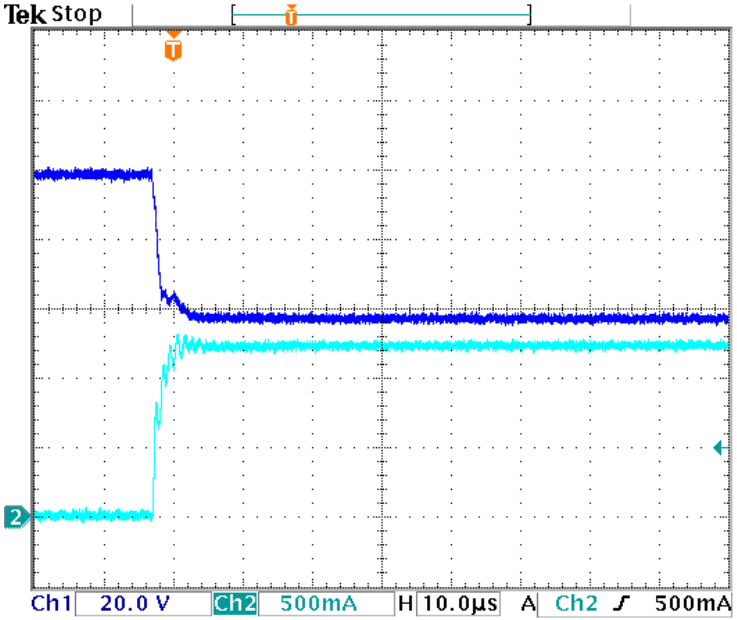


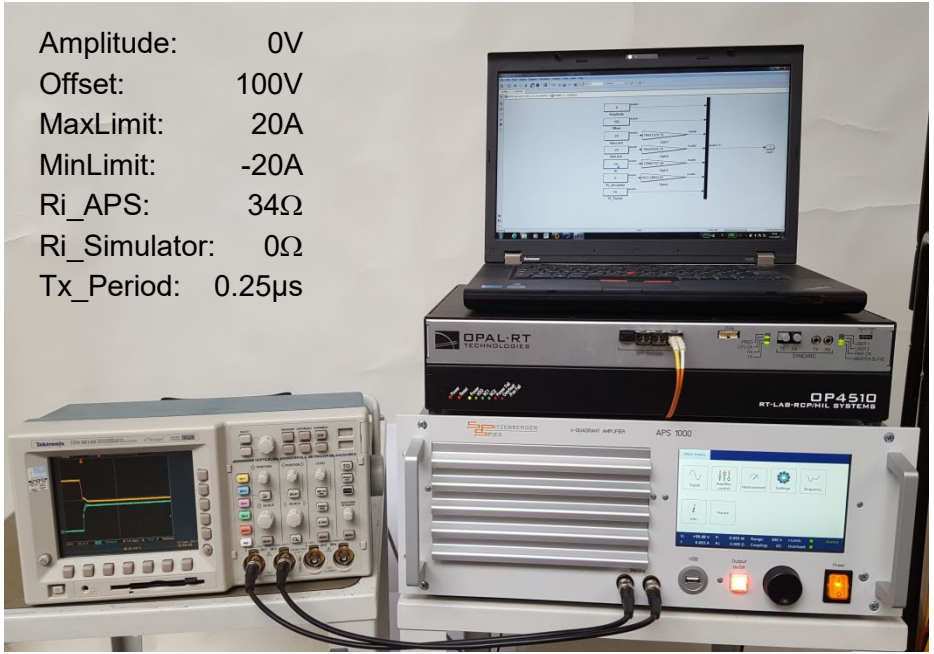
Simulation of internal resistance with RT simulator (0.25µs time steps)





Simulation of internal resistance with power amplifier APS





Conclusion

- Goal: stable and accurate PHIL simulations
- Advantages of linear power amplifiers with analogue interface or especially with optical link:
  - minimized delay time
  - very fast slew rate

  ⇒ high stability and accuracy