

VDA 320 / LV 148

At a glance

Electric and Electronic Components in Motor Vehicles
 48 V On-Board Power Supply
 Requirements and Tests

The relating standards:

VDA 320

LV124

LV148

VOLTAGES

$U_{48r,dyn}$	Lower limit of the dynamic overvoltage range	60 V
U_{48r}	Lower limit of the 2 V tolerance for the dynamic overvoltage range	58 V
$U_{48max,high,limited}$	Maximum voltage of the upper limited operation range	54 V
$U_{48max,unlimited}$	Maximum voltage of the unlimited operation range	52 V
U_{48n}	Rated voltage for 48 V power supply	48 V
$U_{48min,unlimited}$	Minimum voltage of the unlimited operation range	36 V
$U_{48min,low,limited}$	Minimum voltage of the lower limited operation range	24 V
$U_{48stoprotect}$	Storage protection voltage	20 V
U_{48pp}	Peak-to-peak voltage	
U_{48rms}	RMS value of a voltage	
U_{48max}	Maximum voltage that can occur during a test	
U_{48min}	Minimum voltage that can occur during a test	
U_{48test}	Test voltage for 48 V power supply	
U_{12test}	Test voltage for 12 V power supply	14 V
U_{24test}	Test voltage for 24 V power supply	28 V

MODES OF OPERATION

Mode of operation I (MO I):	DUT is not electrically connected
Mode of operation II.a (MO II.a):	The DUT is operated without an operating load
Mode of operation II.b (MO II.b):	The DUT should be operated with the minimum operating load
Mode of operation II.c (MO II.c):	The DUT is operated with the maximum operating load

FUNCTIONAL STATUSES

A	The DUT must perform all the functions.
B	The DUT must perform all the functions while the test parameters are applied; however, one or more functions may lie outside the tolerance indicated for functional status A. The permissible deviations are defined either in the drawing or in the component specifications. After application is terminated, the DUT must return to functional status A automatically.
C	The DUT fails to perform one or more functions while the test parameters are applied. After application is terminated, the DUT returns automatically to functional status A or B (depending on the test). A DUT that acquires undefined functions at any time does not correspond to functional status C.
D	The DUT fails to perform one or more functions while the test parameters are applied. After application is terminated, the DUT returns to functional status A when the terminal is switched off and then on or when the vehicle is restarted. A DUT that acquires undefined functions at any time does not correspond to functional status D.
E	The DUT fails to perform one or more functions while the test parameters are applied; the DUT does not ignite (pursuant to UL 94 v0) and no short circuit occurs between the 48 V system and the 12/24 V system. After application is terminated, the DUT can no longer be used unless it is repaired or replaced.

4.1 E48-01a:

Long-term Overvoltage

DUT mode: II.a, II.b, II.c

t_0 Status A ok

t_r 0.1 s

t_1 60 min

t_f 0.1 s

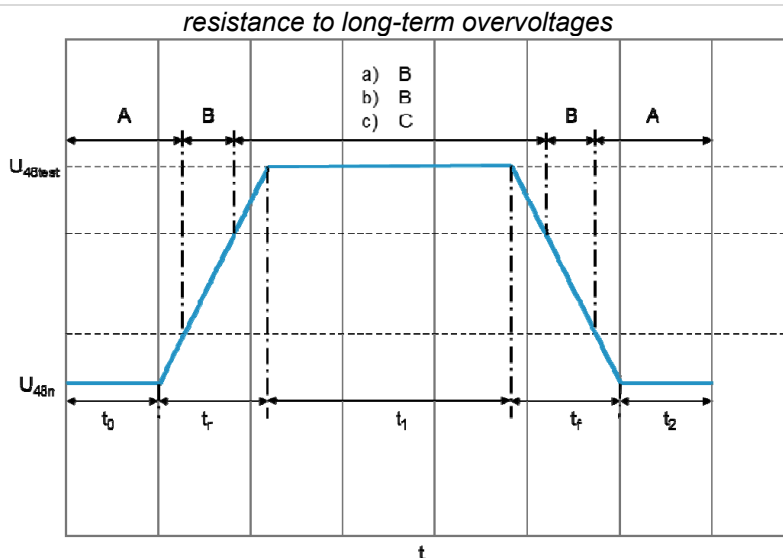
t_2 1 s

U_{48test} $U_{48r,dyn}$ (60V)

T_{test} $T_{max} - 20^\circ\text{C}$

Number of cycles: 1

Number of DUTs: 6



4.2 E48-01b:

Overvoltage with components that return electrical energy

Test part 1

The DUT is connected to a powerful electrical source. The source must not act as a sink while the energy is being returned. A resulting feedback current ≤ 10 mA is permitted. This should be demonstrated by measuring the current.

Component feeds energy into the 48 V supply system, which cannot be absorbed in the vehicle power supply and therefore leads to an increase in the voltage

Test part 2

The DUT is connected to a powerful 4-quadrant amplifier and should be operated at U_1 for at least t_0 . After this, activation of the energy feedback begins and when the DUT's feedback current has reached its maximum, absorption of the returned energy should be terminated abruptly (toff). A resulting feedback current ≤ 10 mA is permitted. This should be demonstrated by measuring the current.

DUT Mode: II.c

T_{test} T_{min}, T_{RT}, T_{max}

U_1 $U_{48max,unlimited}$ (52V)

U_2 U_{48r} (58V)

U_3 $U_{48max,high,limited}$ (54V)

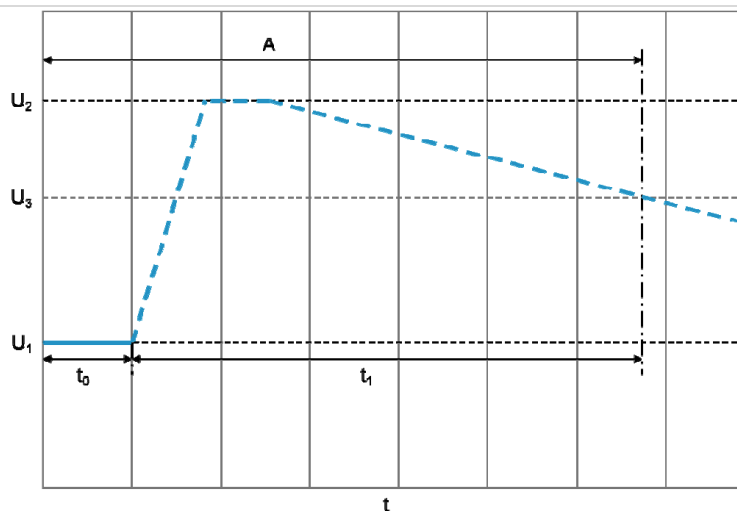
t_0 ≥ 1 s

t_1 ≤ 300 ms

t_{off} ≤ 10 μs

Number of cycles: 3 cycles at all 3 temperatures

Number of DUTs: 6



The time from exceeding the voltage U_1 to falling below the voltage U_3 should be determined and must not exceed t_1

4.3 E48-02:

Transient Overvoltage

DUT Mode: II.c

U_0 U_{48n} (48V)

U_1 70V

U_2 U_{48r} (58V)

t_0 100 ms

t_r 1 ms

t_1 40 ms

t_f 1 ms

t_2 600 ms

t_{3a} 2.5 s

t_{3b} 9 s

R_i $10m\Omega \leq R_i \leq 100m\Omega$

Number of cycles:

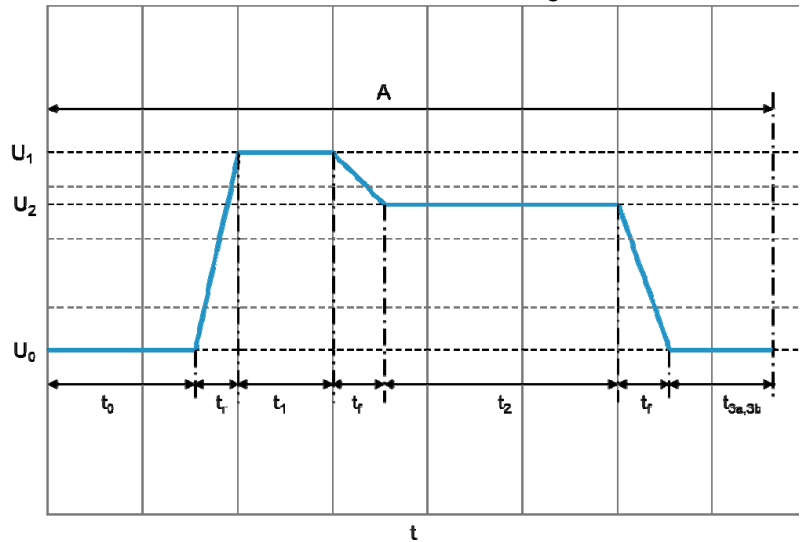
1. Short test: 3x mit t_{3a}

2. Endurance test: 1000x t_{3b}

The two tests are carried out in sequence.

Number of DUTs: 6

Transient overvoltages can occur in the 48 V power supply. This test simulates such overvoltages.



4.4 E48-03:

Transient Event in Lower Limited Operation Range

DUT Mode: II.c

U_0 $U_{48min,unlimited}$ (36V)

U_1 $U_{48min,low,limited}$ (24V)

t_0 60 s

t_f 2 ms

t_1 500 ms

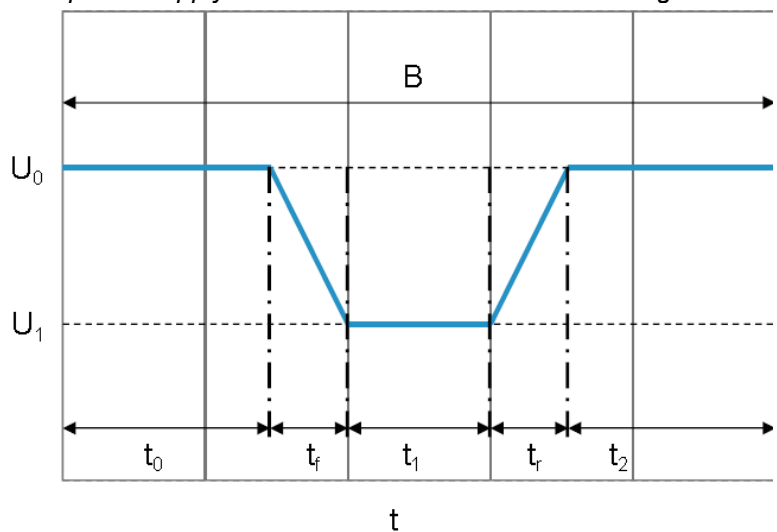
t_r 2 ms

t_2 500 ms

Number of cycles: 1

Number of DUTs: 6

Switching on loads can cause transient undervoltages in the vehicle power supply. This test simulates such undervoltages.

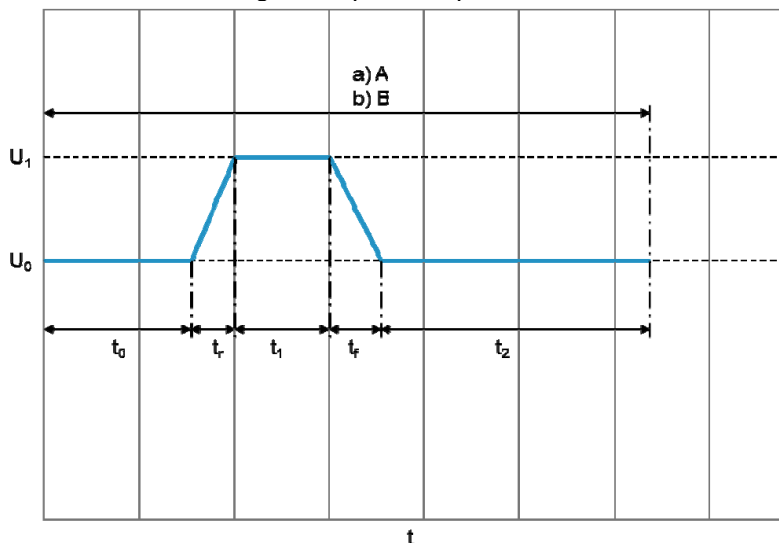


4.5 E48-04:

Recuperation

DUT Mode: II.c	
U_0	$U_{48max,unlimited}$ (52V)
U_1	$U_{48max,high,limited}$ (54V)
t_0	60 s
t_r	100 ms
t_1	60 s
t_f	100 ms
t_2	60 s
Number of cycles: 1	
Number of DUTs: 6	

This test models a longer recuperation phase.

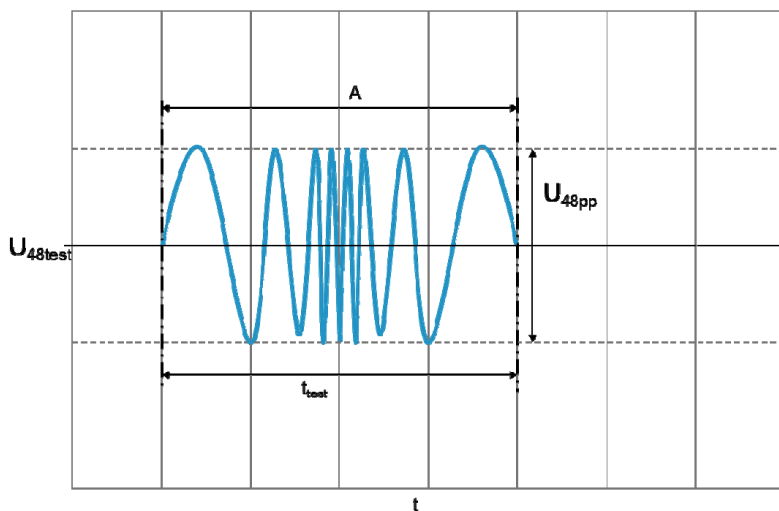


4.6 E48-05:

Superimposed Alternating Voltage

DUT Mode: II.c	
R_i	$\leq 60m\Omega$
U_{48test}	Test 1: $U_{48min,unlimited}$ (36V) Test 2: $U_{48max,unlimited}$ (52V)
t_{test}	30 min
f	F1: 15Hz ... 30kHz F2: 30kHz ... 200kHz
Wobble- Periode	2 min
Wobble- Art	Triangle, logarithmic
U_{48pp}	F1: $6V \pm 2\%$ F2: $2V \pm 2\%$
Number of DUTs: 6	

Alternating voltages can be superimposed on the vehicle power supply. The superimposed alternating voltage can occur at any time during generator operation. This situation is simulated in this test.

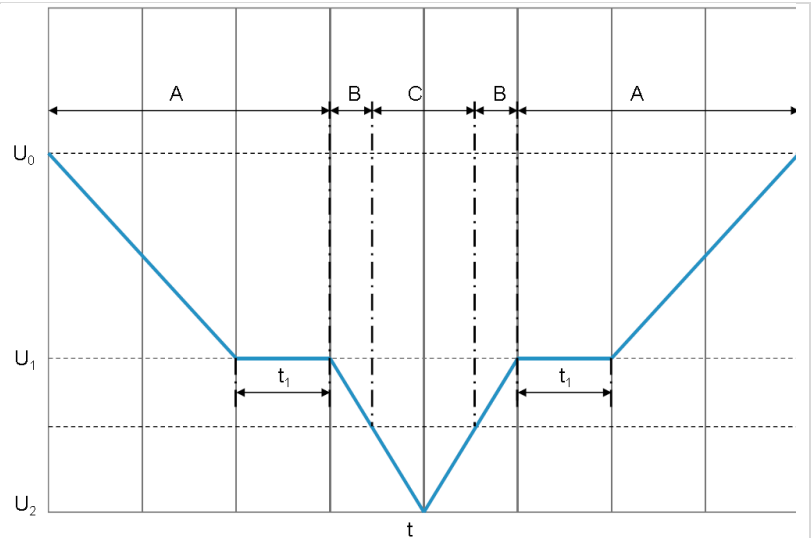


The ripple-voltage U_{48pp} is to be set before connection to DUT.

4.7.1 E48-06a:

Slow decrease and increase of the supply voltage for operation without storage:

DUT Modes: II.a, II.c	
U_0	$U_{48\max, \text{unlimited}}$ (52V)
Voltage gradient	$\pm 2\text{V/min}$
U_1	$U_{48\min, \text{unlimited}}$ (36V)
U_2	0V
t_f	Until the error memory has been read out completely
Number of cycles: 1 (II.a), 1 (II.c)	
Number of DUTs: 6	



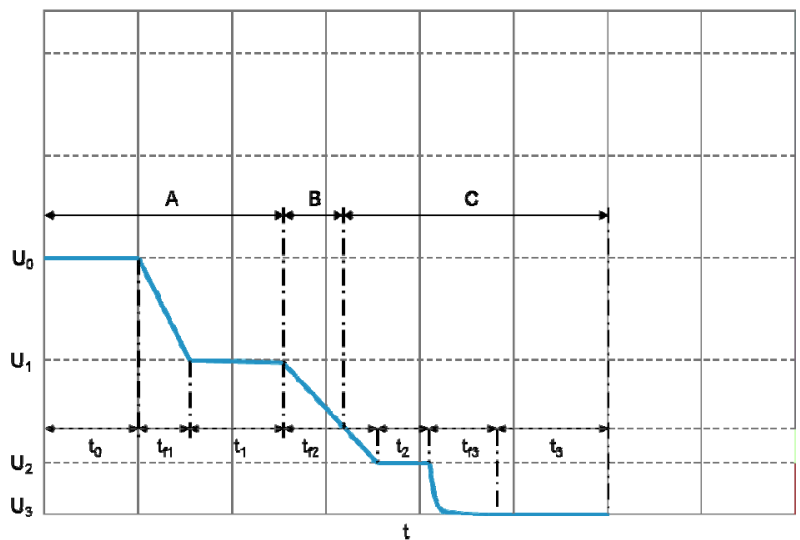
The test investigates slow decrease and increase of the supply voltage, as occurs during slow discharging and charging processes.

4.7.2 E48-06b:

Slow decrease and increase of the supply voltage for operation without storage Part 1:

DUT Mode: II.a	
U_0	$U_{48\max, \text{unlimited}}$ (52V)
U_1	$U_{48\min, \text{unlimited}}$ (36V)
U_2	$U_{48\text{stopprotect}}$ (20V)
U_3	0V
t_0	100 ms
t_{f1}	8 min
t_1	$\geq 60\text{ s}$ (during this phase the error memory is read out)
t_{f2}	8 min
t_2	60 s
t_{f3}	3 s
t_3	60 s
Number of cycles: 1	
Number of DUTs: 6	

The test investigates slow decrease of the supply voltage to the storage protection voltage, after which the storage is disconnected.

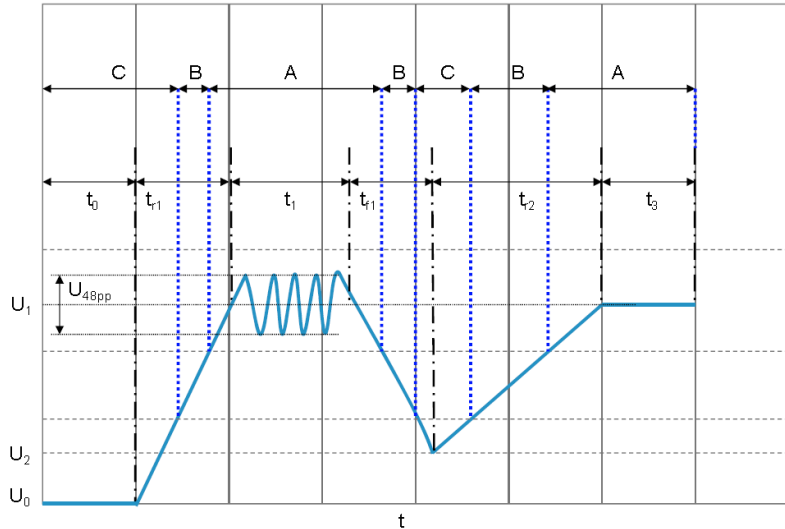


4.7.3 E48-06c:

Slow decrease and increase of the supply voltage for operation without storage Part 2:

DUT Mode: II.b after the final voltage has been reached

R_i	$\leq 60 \text{ m}\Omega$
U_0	0V
U_1	U_{48n} (48V)
U_{48pp}	6V at 10kHz
U_2	$U_{48stopprotect}$ (20V)
t_0	100 ms
t_{r1}	300 ms
t_1	$\geq 60 \text{ s}$ (during this phase the error memory is read out)
t_{r1}	1 ms
t_{r2}	14 min
t_3	100 ms
Number of cycles: 1	
Number of DUTs: 6	



The test examines connection of the generator while the storage is disconnected, followed by connection of the discharged storage.

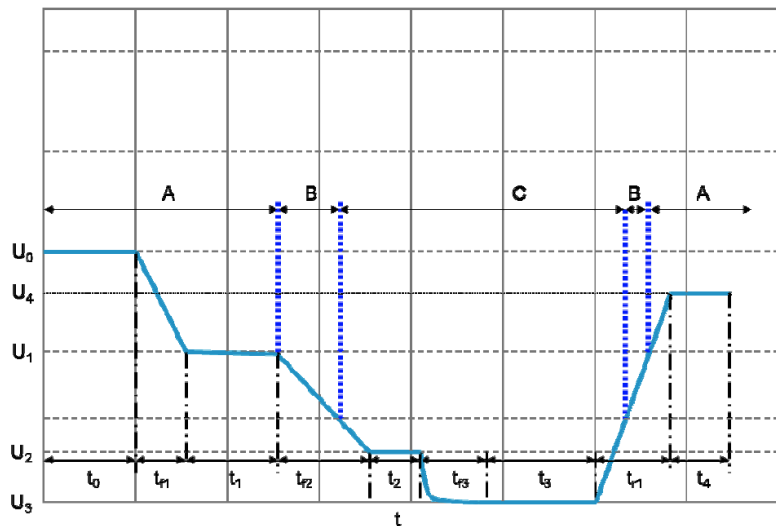
4.8 E48-07:

Slow decrease and abrupt increase of the supply voltage

DUT Mode: II.a

U_0	$U_{48max,unlimited}$ (52V)
U_1	$U_{48min,unlimited}$ (36V)
U_2	$U_{48stopprotect}$ (20V)
U_3	0V
U_4	U_{48n} (48V)
t_0	100 ms
t_{r1}	8 min
t_1	$\geq 60 \text{ s}$ (during this phase the error memory is read out)
t_{r2}	8 min
t_2	60 s
t_{r3}	3 s
t_3	300 s
t_{r1}	$\leq 100 \text{ ms}$
t_4	100 ms
Number of cycles: 1	
Number of DUTs: 6	

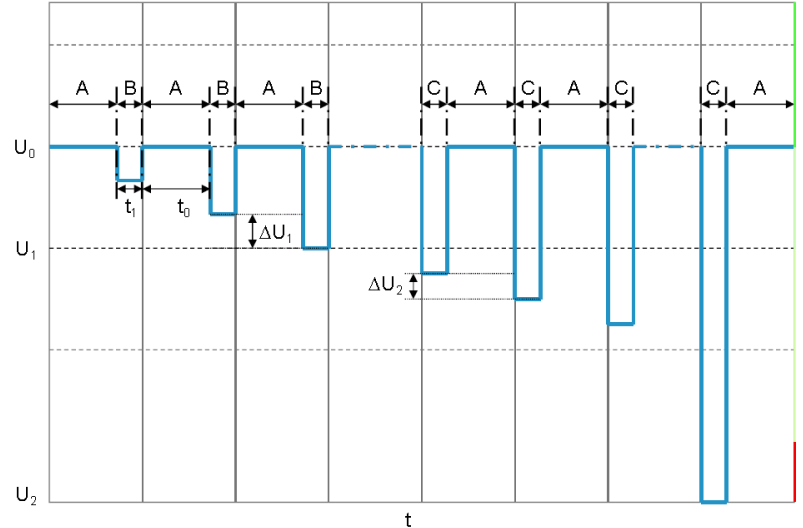
This test simulates slow decrease of the power supply voltage to the storage protection voltage followed by switching off to 0 V and abrupt reapplication of the storage voltage by means of either a charged storage or a new storage.



4.9 E48-08: Reset behaviour

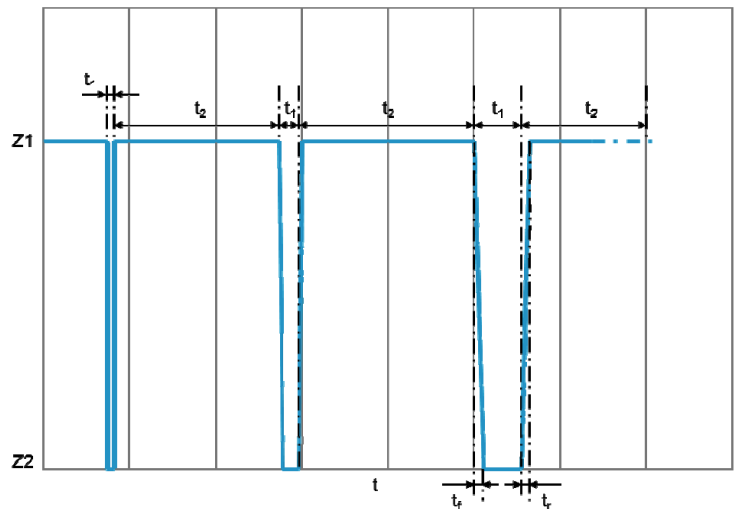
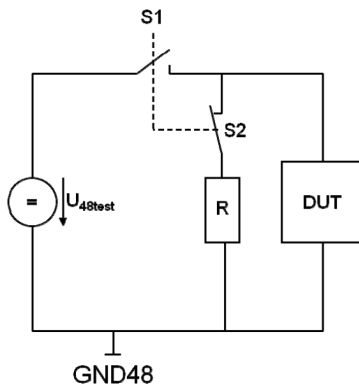
DUT Mode: II.c	
U_0	$U_{48min,unlimited}$ (36V)
ΔU_1	2V (Range from U_0 to U_1)
U_1	$U_{48min,low,limited}$ (24V)
ΔU_2	0.5V (Range from $U_{48min,low,limited}$ to 0V)
U_2	0V
t_0	At least 10 s and until the DUT has regained 100% operability
t_1 –	Test 1: 5s
t_1 –	Test 2: 100 ms
$t_{f/r}$	≤ 100 ms
t_4	100 ms
Number of cycles: 1	
Number of DUTs: 6	

The reset behaviour of a component (control device logic is supplied by the 48 V system) in its environment is modelled and tested.



Two different test sequences are required to simulate a range of poweroff times.
A component has always to undergo both sequences.

4.10 E48-09: Brief Interruptions



The behaviour of the component when subjected to brief interruptions of varying duration is tested. In each case one reference measurement should be performed and documented with $1\text{ k}\Omega$ ($\pm 5\%$) and one with $10\text{ }\Omega$ ($\pm 5\%$) as a DUT substitute. Verification of the steepness of the slope should be provided with this set-up. Low-inductance components should be used as resistors.

DUT mode of operation	Mode II.c								
Test set-up	Basic circuit according to Figure 15. The modelling of the vehicle power supply should be agreed with the client's specialist department.								
R_i	$\leq 60 \text{ m}\Omega$ incl. switch S1								
R	$\leq 100 \text{ m}\Omega$ total resistance incl. layout of wiring harness and switch S2								
Z1	S1 closed and S2 open								
Z2	S1 open and S2 closed								
$U_{48\text{test}}$	U_{48n}								
t_1	The supply voltage of $U_{48\text{test}}$ is interrupted at varying intervals in the following sequence: <table border="1"> <tr> <td>100 μs to 1 ms</td><td>100 μs intervals</td></tr> <tr> <td>1 ms to 10 ms</td><td>1 ms intervals</td></tr> <tr> <td>10 ms to 100 ms</td><td>10 ms intervals</td></tr> <tr> <td>100 ms to 2 s</td><td>100 ms intervals</td></tr> </table>	100 μs to 1 ms	100 μs intervals	1 ms to 10 ms	1 ms intervals	10 ms to 100 ms	10 ms intervals	100 ms to 2 s	100 ms intervals
100 μs to 1 ms	100 μs intervals								
1 ms to 10 ms	1 ms intervals								
10 ms to 100 ms	10 ms intervals								
100 ms to 2 s	100 ms intervals								
t_2	$> 10 \text{ s}$ The test voltage $U_{48\text{test}}$ must be maintained at least long enough for the DUT to become 100% operational again (all systems have restarted perfectly).								
t_f	$\leq 10 \mu\text{s}$								
t_r	$\leq 10 \mu\text{s}$								
Number of cycles	1								
Number of DUTs	6								

4.11 E48-10: Starting Pulses

DUT Mode:

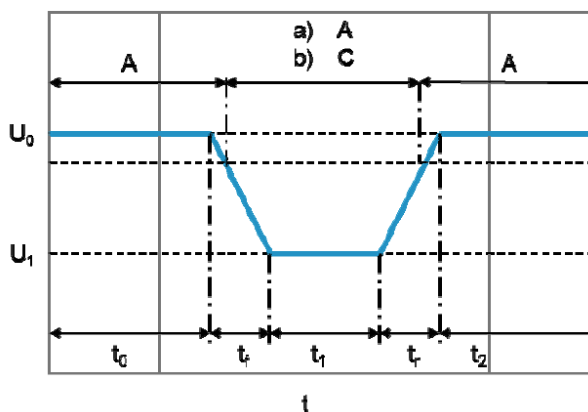
II.C For components relevant to starting
II.b For components not relevant to starting

Test pulse 'normal' and 'severe'

U_0	U_{48n} (48V), cold start normal 40V, cold start severe
U_1	$U_{48\text{min,low,limited}}$ (24V)
t_0	2 s
t_f	1 ms
t_1	1 s
t_r	1 ms
t_2	2 s

Number of cycles: 10

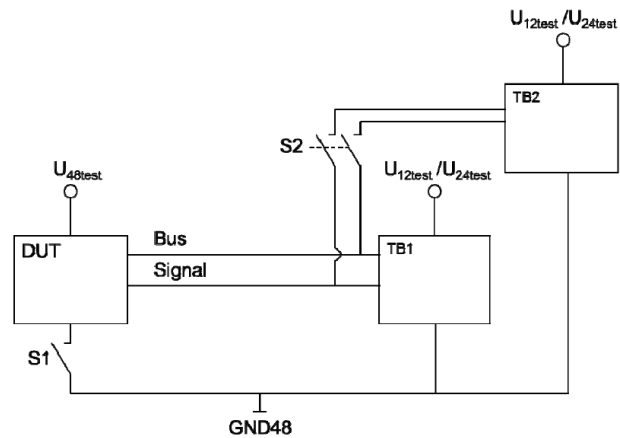
Number of DUTs: 6



In the case of a cold start (starting the engine), the storage voltage falls to a low value for a short period, after which it rises again.

4.12 E48-11: Ground Loss in 48 V Power Supply (BN48)

DUT Mode: II.c	
U_{48test}	U_{48n} (48V)
t_{test}	see tests
T_{test}	$T_{max} - 20^{\circ}\text{C}$
Number of cycles: 1	
Number of DUTs: 6	



Test 1:

$S1$ closed, $S2$ closed, all the components DUT/TB1/TB2 function perfectly.
 $S2$ is opened.

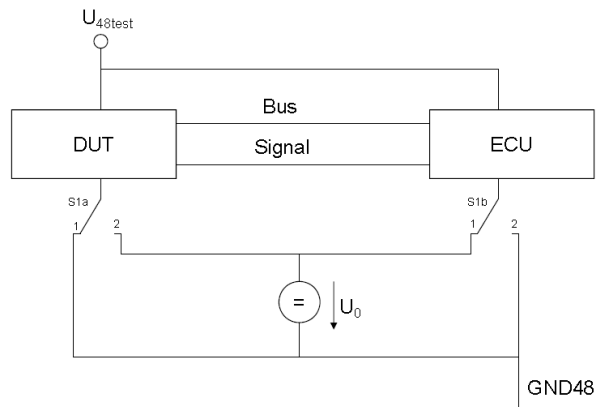
Test 2:

$S1$ closed, $S2$ closed, all the components DUT/TB1/TB2 function perfectly.
 $S1$ is opened. The test lasts for 30 minutes after $S1$ is opened.

The test simulates a loss of ground by a component in the 48 V power supply system, which is supplied solely from the 48 V system and has interfaces to 12/24 V components.

4.13 E48-12: Ground Offset

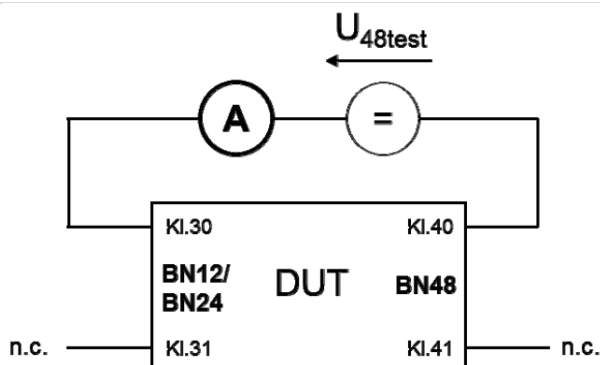
DUT Mode: II.c	
U_{48test}	U_{48n} (48V)
U_0	1.0 V
Number of cycles: 1	
Number of DUTs: 6	



If the DUT has several voltage and ground connections for the 48 V power supply, the test must be performed separately for each connection point. In general, a ground offset of ± 1.0 V should be taken into consideration when dimensioning the interface between two components.
The component is connected as shown in above figure.

4.14 E48-13: Internal Dielectric Strength

DUT Mode: I.a	
U_{48test}	$U_{48r,dyn}$ (60V)
t_{test}	60 min
F_{rel}	50%
T_{test}	35°C
Number of cycles: 1	
Number of DUTs: 6	



Tst points:

Application of the test voltage between

— both supply connections,

— additional test points agreed with the relevant client department.

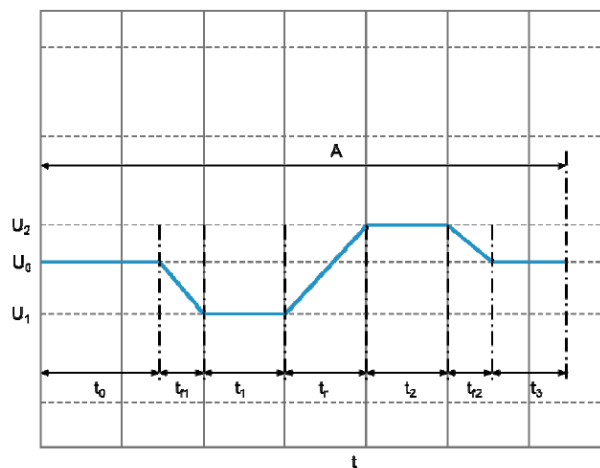
E48-14: Standby Current

DUT Mode: II.a	
U_{48test}	U_{48n} (48V)
T_{test}	T_{min} , T_{RT} , T_{max}
Number of DUTs: 6	

Test condition	Temperature range	Max. standby current
	T_{min} to 40 °C	0,1 mA
	40 °C to T_{max}	0,2 mA

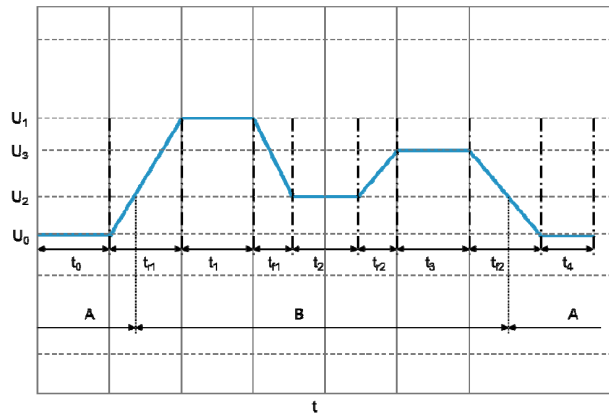
E48-15: Operation in Unlimited Operation Range

DUT Mode: II.c	
U_0	U_{48n} (48V)
U_1	$U_{48min,unlimited}$ (36V)
U_2	$U_{48max,unlimited}$ (52V)
t_0	100 ms
t_{r1}	1 ms
t_1	1 s
t_r	1 s
t_2	10 s
t_{r2}	1 s
t_3	100 ms
T_{test}	T_{min} , T_{RT} , T_{max}
Number of cycles: 10	
Number of DUTs: 6	



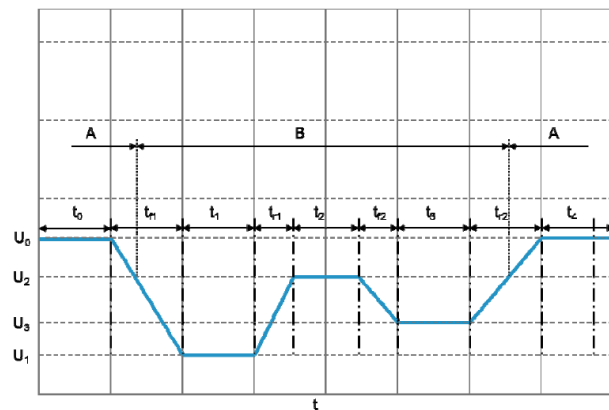
E48-16:
Operation in Upper Limited Operation Range

DUT Mode: II.c	
U_0	U_{48n} (48V)
U_1	$U_{48max,high,limited}$ (54V)
U_2	$U_{48max,unlimited}$ (52V)
U_3	$U_{48max,unlimited} + 1V$ (53V)
t_0	100 ms
t_{r1}	4 s
t_1	10 s
t_{f1}	2 s
t_2	10 s
t_{r2}	2 s
t_3	10 s
t_{f2}	2 s
t_4	100 ms
T_{test}	T_{min}, T_{RT}, T_{max}
Number of cycles: 10	
Number of DUTs: 6	



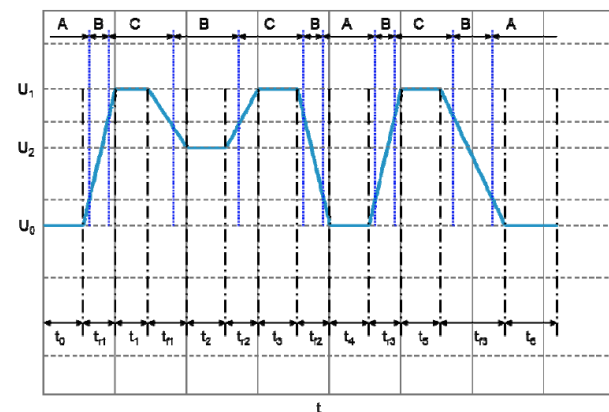
E48-17:
Operation in Lower Limited Operation Range

DUT Mode: II.c	
U_0	U_{48n} (48V)
U_1	$U_{48min,low,limited}$ (24V)
U_2	$U_{48min,unlimited}$ (36V)
U_3	$U_{48min,low,limited} + 1V$ (25V)
t_0	100 ms
t_{r1}	4 s
t_1	10 s
t_{f1}	2 s
t_2	10 s
t_{r2}	2 s
t_3	10 s
t_{f2}	2 s
t_4	100 ms
T_{test}	T_{min}, T_{RT}, T_{max}
Number of cycles: 10	
Number of DUTs: 6	



E48-18:
Overvoltage Range

DUT Mode: II.c	
U_0	U_{48n} (48V)
U_1	U_{48r} (58V)
U_2	$U_{48max,unlimited} + 1V$ (53V)
t_0	100 ms
t_{r1}	10 ms
t_1	1 s
t_{f1}	1 s
t_2	10 s
t_{r2}	1 ms
t_3	2 s

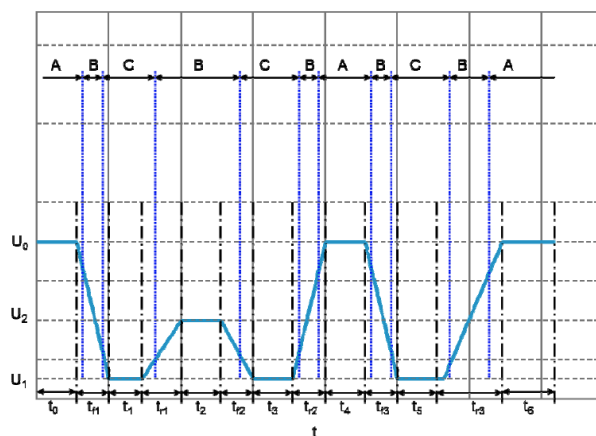


t _{f2}	1 s
t ₄	5 s
t _{r3}	10 s
t ₅	2 s
t _{f3}	10 s
t ₆	100 ms
T _{test}	T _{min} , T _{RT} , T _{max}
Number of cycles: 10	
Number of DUTs: 6	

E48-19:

Undervoltage Range

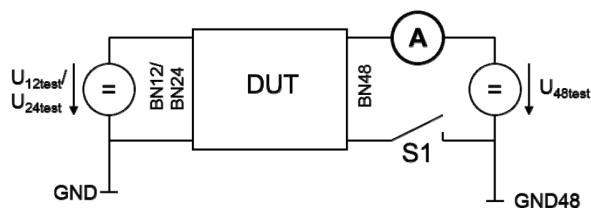
DUT Mode: II.c	
U ₀	U _{48n} (48V)
U ₁	U _{48stop} protect (20V)
U ₂	U _{48min,low,limited} +1V (25V)
t ₀	100 ms
t _{f1}	1 s
t ₁	1 s
t _{r1}	10ms s
t ₂	10 s
t _{f2}	1 s
t ₃	2 s
t _{r2}	1 ms
t ₄	5 s
t _{f3}	10 s
t ₅	2 s
t _{r3}	10 s
t ₆	100 ms
T _{test}	T _{min} , T _{RT} , T _{max}
Number of cycles: 10	
Number of DUTs: 6	



E48-20a:

Fault Current, Part 1

DUT Mode: II.a	
Test set-up see figure	
U _{48test}	a) U _{48n} (48V)
	b) U _{48r,dyn} (60V)
t _{test}	10 min
T _{test}	T _{RT}
Number of cycles: 1	
Number of DUTs: 6	

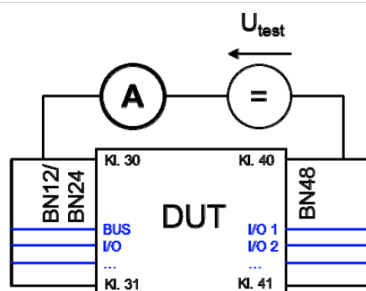


For the terminal 40 supply current: $|I| \leq 1 \mu A$

E48-20b:

Fault Current, Part 2

DUT Mode: II.a	
Test set-up see figure	
U _{48test}	a) U _{48n} (48V)
	b) U _{48r,dyn} (60V)
t _{test}	10 min
T _{test}	T _{RT}
Number of cycles: 1	



Number of DUTs: 6

For the current between the 12/24 V and 48 V systems:
 $|I| \leq 1 \mu A$

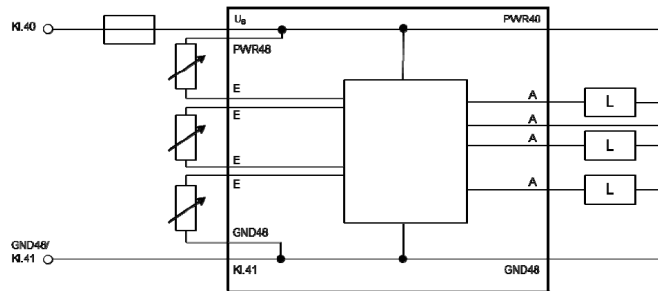
E48-21:

Short Circuit in Signal Line and Load Circuit

Short circuits on all 48 V system device inputs and outputs are examined, as are short circuits in the 48 V system load circuit. Any 12/24 V part present is not tested. All 48 V supply system inputs and outputs should be designed to be short-circuit proof with respect to the test voltage and GND48.

The following tests should be performed:

- ☐ with activated and non-activated outputs,
- ☐ without voltage supply,
- ☐ without ground connection.



L: Load E: Input A: Output
PWR48: Output U_B /KI.40 GND48: Input/ Output KI.41
 U_B : BN48 power supply of the DUT

DUT mode of operation	Mode II.c
Test duration	Short circuit of each 48 V system pin individually for 60 s to test voltage and GND48
Test voltage	$U_{48max,unlimited}$ and $U_{48min,unlimited}$
Test set-up	The power supply used for the test must be able to supply the short-circuit currents expected from the component.
Number of cycles	Each pin, once against the test voltage/terminal 40 and once against GND48/ terminal 41
Number of DUTs	6